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ON
DC TO DC CONVERTER,
ENGINEERED MAGNETICS MODEL EMCR131
(NASA CONTRACT NO. NAS5-3470
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First Quarterly Report, 1 July 1963 - 1 Oct. 1963

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TABLE OF CONTENTS

SUMMARY AND CONCLUSION

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This report covers the first phase of design of a high efficiency DC to DC Converter with 59 watts output from four regulated isolated and short circuit protected outputs. Efficiency goals are:

1. 85% efficiency at full load (59 watts) for all input line voltages from 12 to 20 volts.
2. 80% efficiency at minimum load (12 watts) for all input voltages from 12 to 20 volts.

Other design goals pose no difficult problems and are attainable.

Chief obstacles to achieving high efficiency are associated with transistor charge storage and diode loss in output rectification circuits.

At this time, it appears the desired high line efficiency will be achieved with little difficulty. Efficiencies under other conditions will be close to the design goal. It is anticipated that transistor loss can be maintained satisfactorily low with recently developed transistors and optimum circuitry. Reduction in diode loss is being sought through fast recovery diodes or transistors used as synchronous rectifiers. No completely satisfactory solution has been found and this remains a major problem.

Breadboard tests have verified circuit operation where this was considered desireable.

AUTHOR

I. INTRODUCTION This report describes the first quarterly period of effort to develop a DC-DC Converter of very high efficiency. The converter is to be powered from a solar-cell-battery combination power source. High efficiency and reliability are prime goals of the study. The converter has four isolated outputs with individual short-circuit protection on each output. Each output must meet regulation, ripple, and dynamic impedance requirements that necessitate separate regulation in each output. It is desired to attain the highest efficiency at maximum input voltage. The work performed during the period covered of this report consisted of a study of overall "block diagram" approaches, the construction of an oscillator and pulse width regulator sections, and an extensive search to find a transistor suitable for use as a synchronous rectifier.

II. DISCUSSION

A. Overall Approach: The first phase of the effort consisted of a theoretical evaluation of the possible overall approaches to the design. Each approach was evaluated with respect to the various requirements of the design specification. The desired high reliability dictated that the complexity of the circuit be kept at a minimum. With this in mind, the other electrical requirements that were most significant in determining the design approach were the specified minimum load and the required maximum efficiency at maximum input voltage.

Block diagrams of five design approaches that were considered are as shown in Figures 1 through 5. A discussion of each approach 1 through 5 corresponds to Figures 1 through 5.

1. This approach uses a pulse width regulator to supply a regulated voltage to a Transistor Saturable Reactor Oscillator. The input voltage to the oscillator would be controlled to about ±3% over the input voltage range of 12 to 20 volts. After rectification, the output of the oscillator is fed through a

series regulator supplying the unit outputs. Load current sensing for overload protection is accomplished by means of a current transformer in the secondary winding of the power transformer in the oscillator. Since isolation is required between each of the unit outputs, a separate series regulator and current sense transformer are required for each of the four outputs. The series regulator is required to meet the regulation and dynamic response specification. This approach was felt to be undesirable. The efficiency would be lowest at high input voltage. Since the pulse width regulator cannot supply a higher voltage than its input voltage, the oscillator would have to be designed for an input voltage of about one-half volt less than the minimum line input voltage or approximately 11.5 volts. A pulse width regulator uses a "commutating" or "free wheeling" diode to allow the choke to discharge into the load when the series switch is opened. See circuit diagram included in Figure 1. The percentage of time that this diode is conducting is approximately equal to one minus the output voltage of the regulator divided by the input voltage to the regulator. During this period of diode conduction, the power being fed to the oscillator is coming from a source whose voltage is equal to the input voltage of the oscillator plus the diode drop, i.e., the drop across the choke. This drop would be 12.5 volts (assuming a 1 volt diode drop) in this case. The loss in the diode would be 1/12.5 or 8%. At high line, the diode would be conducting $1-\frac{11.5}{20} = 1- .575 = 42.5\%$ of the time. At high line for 42.5% of the time, there would be a loss of 8% due to the regulator commutating diode alone. Other circuit losses would also be maximized by this approach. Since a saturated transistor exhibits approximately a linear saturation resistance as a function of collector current, the losses in the collector circuit of the oscillator switching transistors are essentially $I_c^2 Rsat$. The input voltage times input current to the oscillator

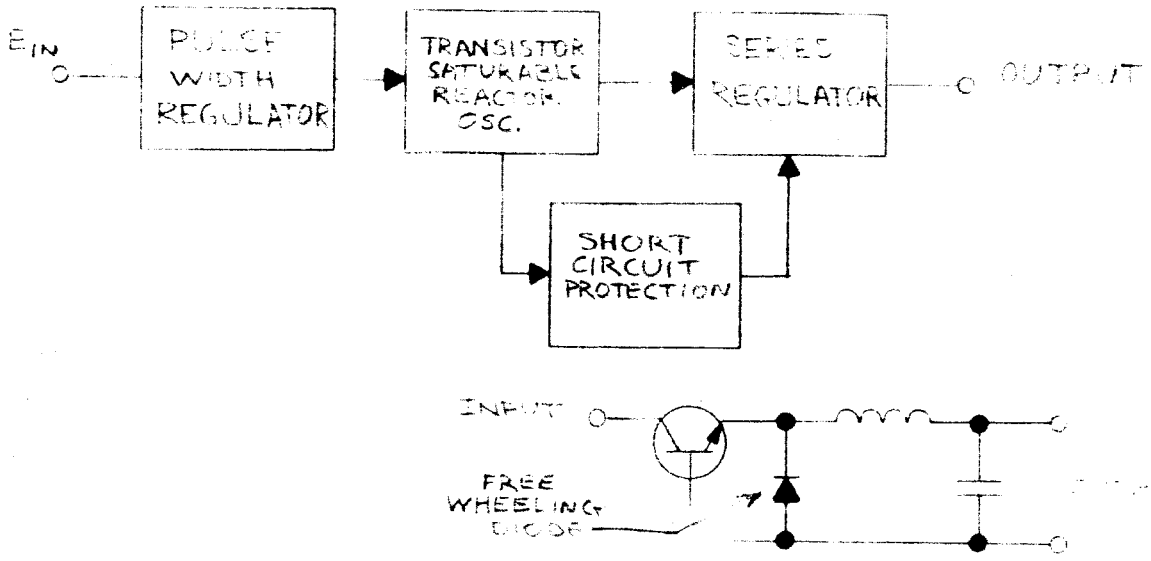


FIGURE 1. BLOCK DIAGRAM OF APPROACH 1.

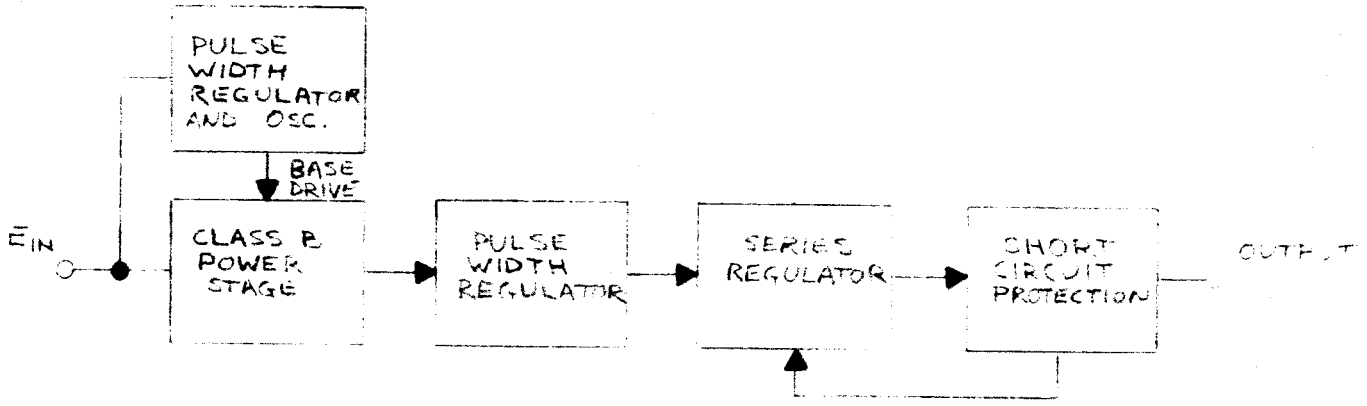


FIGURE 2. BLOCK DIAGRAM OF APPROACH 2.

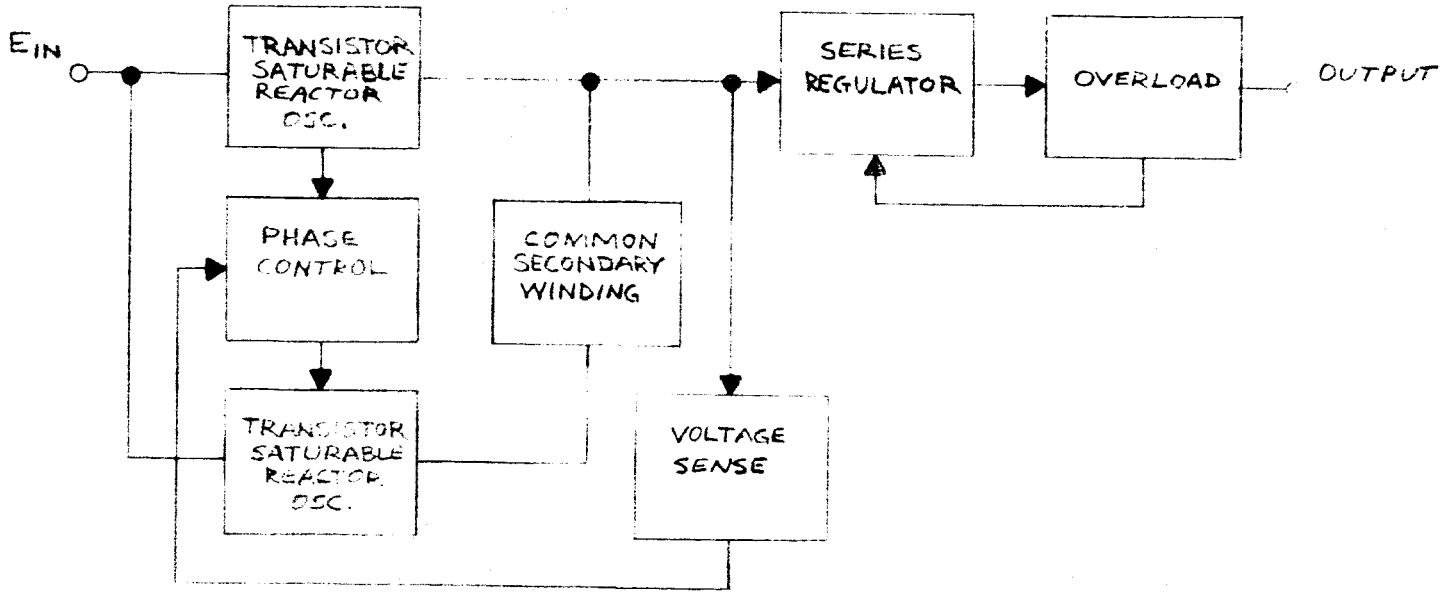


FIGURE 3. BLOCK DIAGRAM OF APPROACH 3.

must equal the output power divided by the efficiency. The lower the input voltage to the oscillator, the higher will be the switching transistor collector current. As the collector circuit losses are proportional to I_c^2, this can be quite significant. This approach has the oscillator running at a lower input voltage and, hence, a larger input current for a given load than an oscillator running directly from the input source. With the switching transistors operating at higher currents, additional base drive would be required. Base circuit losses would also be higher than an oscillator working at higher input voltage and lower current. However, the base losses would probably not be any larger than most other voltage drive approaches.

Since high efficiency is desired at high line, approach 1 was considered to be undersirable. Also, since the base drive is not a function of input current, efficiency would be very low at light load and high input voltage. It was doubtful whether 85% efficiency could have been obtained under any combination of input voltage and load with this circuit.

2. This approach uses a small power regulator-saturable reactor oscillator to feed base drive to the main power stage. The output voltage of the power stage follows the input voltage. Subsequent to rectification from the power stage, a pulse width regulator feeds a coarse regulated voltage to the output series regulator. In this approach, a separate regulator-oscillator must be used for base drive. This is necessary due to the voltage feed back used to drive the base of the switching transistors. The power consumed to do this is approximately E_b^2/r_b; where E_b is the total voltage being fed back to the base-emmitter circuit and r_b is the base resistor used for base-current temperature stabilization. Without a separate regulator, the circuit would have to be designed to give sufficient i_b and hence E_b for an input voltage of 12 volts. At 20 volts

E_b would be $\frac{20}{12}$ times its required minimum level and the power dissipated in the base circuit would be $(\frac{20}{12})^2$ times as large as at low line. In addition, this design must also provide enough base drive to supply full load at minimum input voltage, so that the base drive current and hence base circuit losses are the same as in approach 1. The small additional power consumed in the base drive oscillator and regulator actually cause this approach to consume slightly more power in base drive than approach 1. The pulse width regulator preceding the series regulator as in approach 1 gives minimum efficiency at high line. The commutating diode does not cause such a high percentage loss in the 50 and 20 volt outputs; but in the two 12 volt outputs the diode causes the same percentage loss as in approach 1. However, in this approach, slightly less than 1/2 the total power is being supplied from the 12 volt outputs whereas in approach 1 all the power from the unit had to be supplied, at 12 volts, from a pulse width regulator. Another drawback to this approach is that load current sensing for short circuit protection must be accomplished in the dc line since the average current in the secondary of the power transformer is a function of input voltage as well as load current. Whereas the drop across the primary of a current transformer can be as low as 0.1 volt, the drop across a sense resistor in a dc line would have to be approximately 0.3 volt to operate a germanium transistor or 0.7 volt to operate a silicon transistor. A 0.7 volt drop in a 12 volt output would represent a $\frac{.7}{12.7}$ or 5.5% loss. When these factors are all considered, it seems improbable that the efficiency goals could be obtained with this approach. Again, as in approach 1, lowest efficiency is at high line. Another disadvantage to this approach is its complexity. Pre-regulation for input voltage variation is required ahead of each series regulator. Thus, four pulse width regulators are required. Each pulse width regulator contains a comparitively

large number of parts. In addition, another regulator and oscillator are required for base drive power and these still do not provide a base drive dependent on overall load. This approach, then, did not appear to offer any apparent advantages with respect to efficiency and the complexity was not consistent with the reliability and overall concept of the specification.

3. This approach uses a variable time delay between two oscillators to effect pre-regulation for input voltage variation. Each oscillator has its own power transformer core and primary windings. The secondary windings are wound common to both cores. In this way the effective output voltages of each of the two oscillators are added or subtracted depending on whether the two oscillators are in-phase or out-of-phase. The net waveform on the secondary windings is a quasi square-wave. The two oscillators are designed identically so that when they are out-of-phase the net secondary voltage is zero. When they are in-phase, the net secondary voltage is twice what it would be if only one of the oscillators were used. The voltage is sensed from one of the secondary windings and is used to control the time relationship between the two oscillators by means of a saturable reactor. As the input voltage increases, the two oscillators become more out-of-phase to give the same average output voltage. After rectification of the secondary voltage, the waveform is similar to that of the pulse width regulator just before the inductor. Thus an L-C filter, with a commutating diode, must be used between the rectification diodes and the series regulator. This gives minimum efficiency at high line. Load current sensing must again be accomplished in the dc output line. Also, a separate regulator-oscillator is needed for base drive since the voltage on the individual windings of each transformer varies with the input voltage. Current feed back

cannot be used with this approach since, during the period of time when the two oscillators are out-of-phase, no collector current is flowing and hence there would be no drive current to sustain oscillation.

This approach would offer good efficiency at low input voltage. However, lower efficiency at high input voltage, losses due to load current sensing in the dc output buss, and the added complexity for the regulated base drive made it appear that this approach was not the optimum one that could be taken.

4. This approach uses a pulse width regulator and a second oscillator to regulate the input voltage to the main power oscillator. Unlike approach 1, this method maintains the input voltage to the main oscillator at a value very near the upper extreme of the input voltage range rather than a value near the lower extreme of the input voltage range. This minimizes the input current to the master oscillator and also the $I_c{}^2 Rsat$ losses in the switching transistors. In addition, the regulator-oscillator section is connected in a boost circuit. It supplies only the additional voltage and power to the main oscillator circuit that the line cannot supply to maintain the input voltage to the main oscillator at high line, i.e. 20 volts. When the input voltage is at high line, no-power is flowing through the regulator-oscillator boost circuit. This part of the circuitry would be consuming a very small amount of power under these conditions. As the input voltage decreases, the output voltage from the regulator-oscillator would increase maintaining a constant input voltage to the main oscillator. When the input voltage is just slightly below high line, the regulator must supply only a small voltage to the boost oscillator. This high ratio between input and output voltage combined with a low output voltage (causing high percentage losses in the commutating diode) is a very inefficient mode for a pulse width regulator.

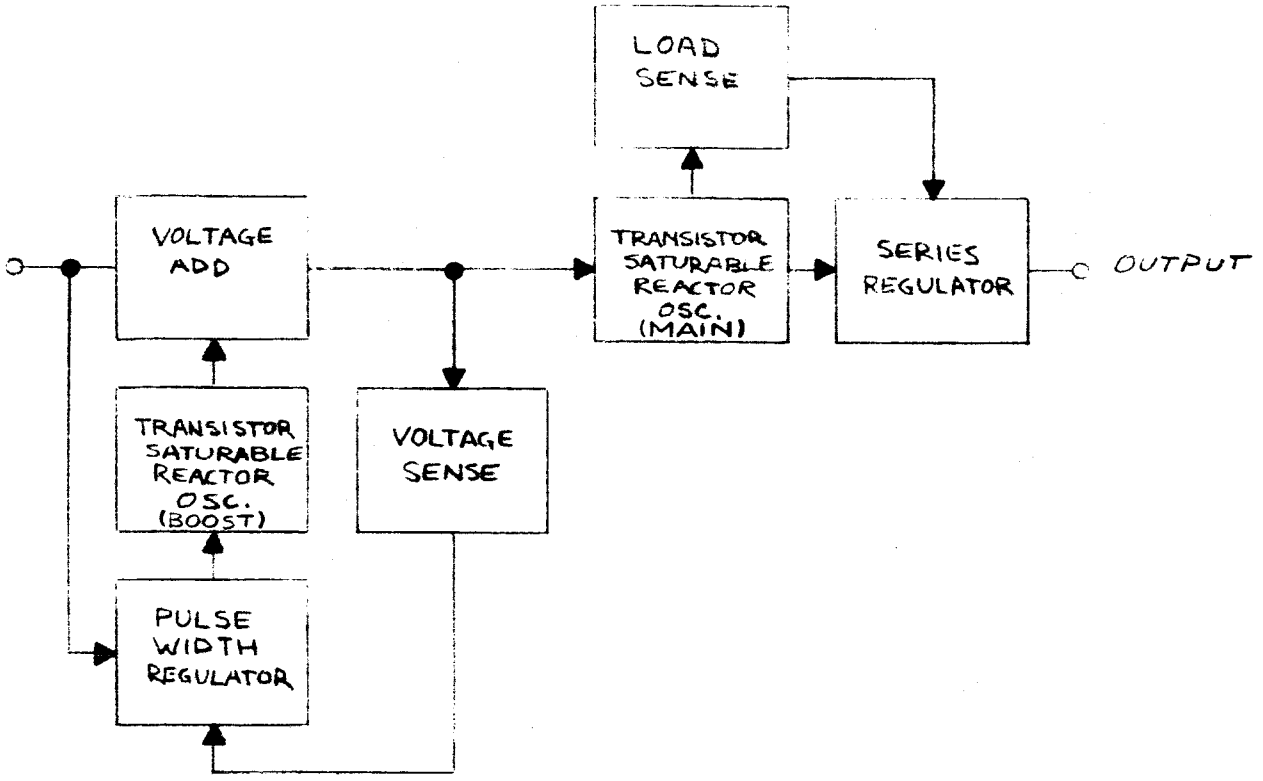


FIGURE 4. BLOCK DIAGRAM OF APPROACH 4.

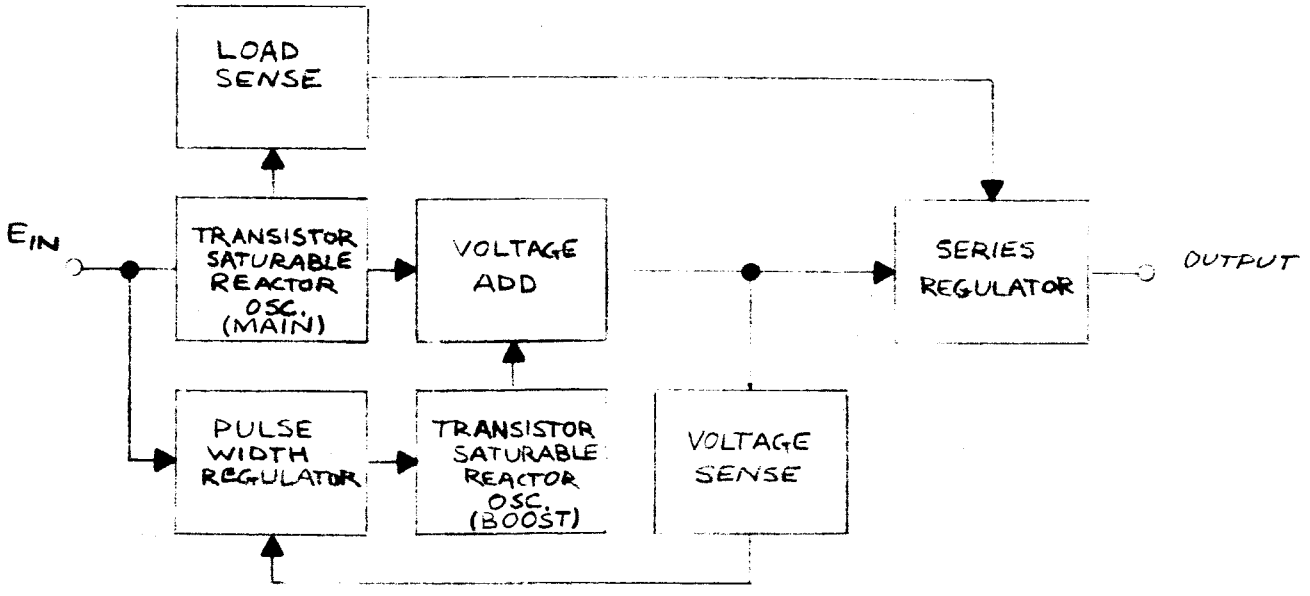
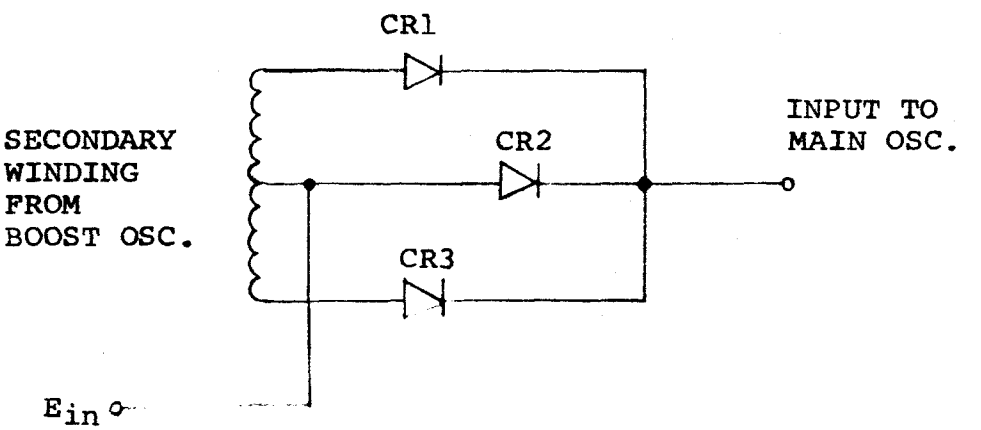


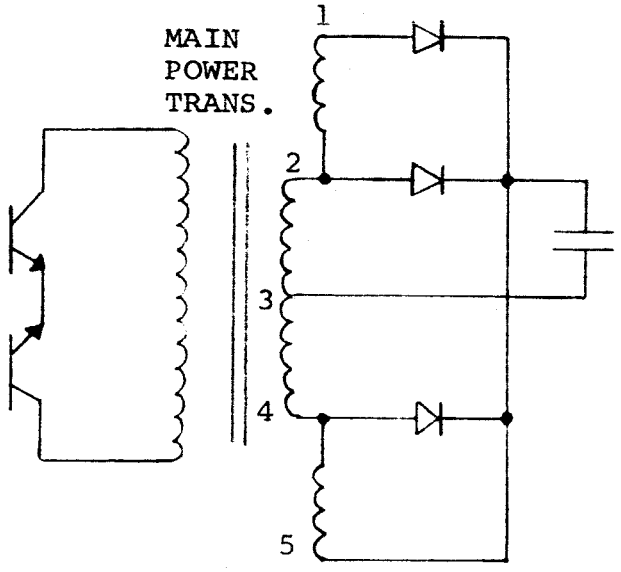
FIGURE 5. BLOCK DIAGRAM OF APPROACH 5.

However, under this condition only a very small amount of the total power of the unit is being supplied through the boost circuit. As the input voltage drops and an increasingly larger percentage of power is supplied by the boost circuit, the voltage difference between input and output of the regulator drops and the output voltage of the regulator rises thus increasing the efficiency of the boost circuit. At minimum input line voltage, the regulator series element is designed to be always "on" elminating the switching and commutating diode losses. Thus, as more and more power is required from the boost circuit, it becomes more efficient in its operation. This approach appears to have many advantages. In addition to favorable efficiency over the entire input voltage range, it allows load current sensing in the ac secondary windings of the power transformer and current feed back in both the main power and boost oscillators. The principal disadvantage to this approach is that the best possible efficiency at high input voltage is not attained. Due to the fact that the input voltage is maintained constant to the main oscillator by means of a conventional boost circuit, the power to the main oscillator must always flow through one diode. The input circuitry is as shown below:



CR2 is required to prevent the shorting of the boost winding when it is operative. At high line, the input current to the main oscillator must flow through CR2. Below high line, the input current flows alternately through CR1 and CR3. Assumption of a 1 volt drop across a silicon diode would result in a 1/21 or approximately 5% loss at this point. In addition, part of the power from the boost circuit comes through the commutating diode in the regulator.

5. This approach is very similiar to approach 4. The only difference is that the boost power is added in an ac mode on the secondary windings of the main power transformer rather than on the dc input line. The circuit used is as shown below.



Windings 1-2 and 4-5 are on boost oscillator transformer.

Windings 2-3 and 3-4 are on main power transformer.

The circuit is designed so that when the input voltage is at its maximum, the main oscillator will supply the full output power. Under this condition, the boost oscillator and pulse width regulator consume an extremely small amount of power.

As the input voltage drops, the boost oscillator adds voltage to the output of the main oscillator. Again, the boost circuit increases in efficiency as the percentage of total power it delivers increases. The boost circuit maintains a coarse regulated voltage (±3%) to the input of the series regulator.

The diodes that are already in the secondary windings are used to prevent shorting of the windings. The power flows only through one pair of diodes at a time. When the boost oscillator is adding voltage at the secondary windings, no current is flowing through the diodes in the main PWR oscillator. In this connection, the power from the input line to the input of the series regulator must flow through one diode only. In approach 4, the power had to flow through a minimum of 2 diodes and, when the boost circuit was operative, part of it had to flow through 3 diodes (including the commutating diode in the regulator). This approach permits for current feed back, load current sensing in the ac lines, minimum possible diode losses, and maximum efficiency at high input voltage. It was thereafter decided to direct total effort to a comprehensive study of this circuit.

In the above discussions current feed back was mentioned as a distinct advantage in those approaches that allowed it. Before commencing with a detailed discussion of approach 5, that was chosen, the advantages of a current feed back oscillator should be emphasized.

Current feed back simply means that the primary winding of a current transformer is placed in the collector circuit of the switching transistors. The secondary is connected base-to-emitter. The base drive current is always a fixed percentage of the collector current. Using only one transformer, the base drive is automatically regulated for the ideal value

over input voltage and load variations. Even when the bases are driven from a regulated voltage source, the regulation is only effective in cancelling variations in the base drive due to input voltage changes. The base drive still does not correct for changes in load. This latter point is extremely significant when using high speed transistors in the oscillators. Even though the switching speed of these transistors is less than 0.1μs, the storage time can be as high as 5 to 6μs. The total time it takes to clear the base region of stored charge is a function of how hard the transistor is overdriven in the "on" condition. With a fixed base drive, independent of load current, the overdrive at a low load is very high. In some cases, the base current might be as much as the collector current. The result is that unless special and relatively complex circuitry is used in the base drive circuit, that at the time of switching, the "off" transistor will turn-on before the "on" transistor turns-off. During the storage time of the "on" transistors, both transistors are on. This results in large current spikes being drawn from the source and a very significant loss of power. In one such oscillator that was operating at 10KC with only moderately fast transistors, the no-load loss was greater than the total losses for 10 watts of output power. The explanation for this is that as the load was increased the overdrive on the switching transistors decreased since the base drive was fixed and the switching losses, due to storage time, decreased faster than copper and transistor "on-time" losses increased. During the first phase of work on this project, the input current was observed on both types of oscillators. Spikes as great as 25 times nominal were observed on the voltage feed back oscillator whereas the current spikes on the current feed back oscillator were only about four times nominal. The savings in base drive power due to lower drive at lower loads is much less than the savings in the collector circuit due to the avoidance of heavy overdriving but power is also saved here.

The reason that current feed back is not used in all converters is that it requires some fixed minimum value of load to be on the converter at all times. This results from the design of the current transformer. The turns ratio is fairly high and is equal to the effective Beta which drives the switching transistors. For example, this ratio might be 15 to 1. Thus, only a few turns are used on the primary to keep the number of secondary turns reasonable. For a core of given circumference, the magnetizing current is inversely proportional to the number of primary turns and the magnetizing current is high for a current transformer with only a few turns on the primary winding. Increasing the size of the core to allow for more turns on both the primary and secondary windings is not a solution since a larger core, being larger in circumference, requires more primary turns to give the same magnitizing current. Using smaller wire to get more turns on the same size core is also not a solution as the resistance of the windings becomes to large. Since the primary of the transformer is in the collector circuit, the resistance must be kept very small. The result is that the current transformer will have a fairly high magnetizing current. No current will be fed back via the secondary winding until the current in the primary winding exceeds the magnetizing current. The collector current should always be greater than approximately five times the magnetizing current of the feed back transformer. One way to avoid this is to have a small amount of voltage feed back that will keep the oscillator operating at light loads. Since the design specification for this project specifies a minimum load, current feed back is possible without any voltage feed back and is the optimum type of drive that can be used.

Once the basic approach was decided upon, the first design that was tried is as shown in Figure 6.

T3 is the main power transformer. T1 is the current feed back transformer for the main oscillator. T2 is the feed back transformer for the boost oscillator. The secondary connections from the two power transformers are for one output only. Four such pairs of secondary are used for the four separate outputs. The operation of the circuit is as follows. See Figure 6.

Upon application of an input voltage, within the specified range, the starting resistor R1 causes either Q1 or Q2 to turn on. Regeneration through the current feed back transformer then causes the main oscillator to begin oscillation. The switching action is initiated by the saturation of T1. T1 is designed to saturate and the saturation time of T1 determines the frequency of the main and boost oscillators. T2 does not saturate. D1, D2 and C1 serve three purposes. First, the diodes allow a high value resistor to be used for a starting resistor since the diodes appear like an open circuit to the starting resistor and no starting current is shunted through them. This minimizes the loss due to the starting resistor. Second, the capacitor provides a negative turn off bias during switching. Since either Q1 or Q2 is always on, there is a dc current flow through D1 and D2 and, hence, a dc voltage across C1 is the polarity shown. C1 maintains this voltage during the switching interval and provides the necessary negative turn off voltage through the respective secondary of the saturated current transformer T1. Third, this network prevents a large unbalance in symmetry in the main oscillator waveform. The period of each half-cycle of operation is determined by the saturation time of T1 for that half-cycle. This is the reason why no resistors are used in the feedback circuit. If resistors were used, the voltage would

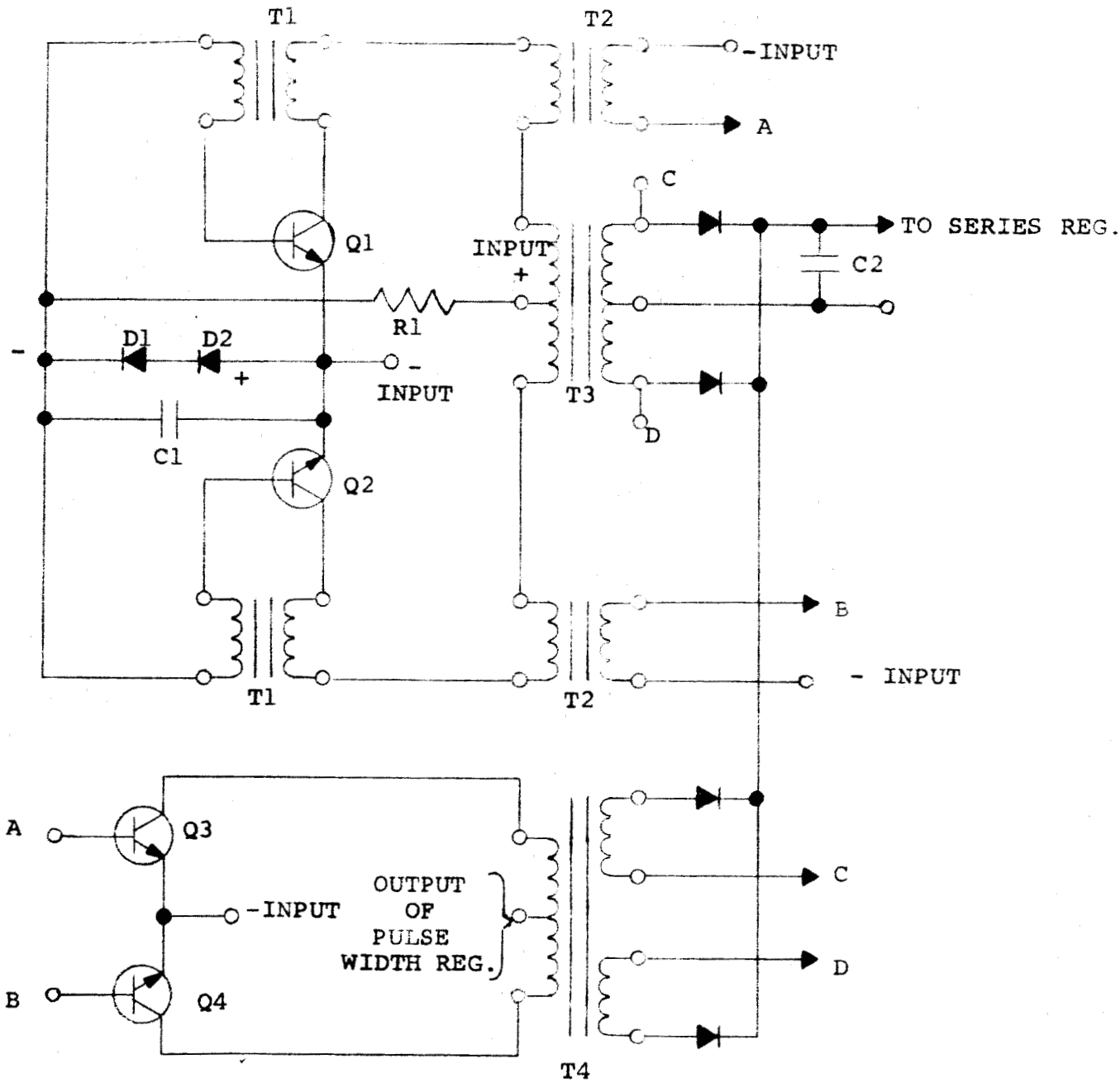


FIGURE 6. MAIN AND BOOST OSCILLATOR CIRCUIT OF APPROACH 5.

rise across the secondary windings of T1 as increased loading would cause increased current flow through the base resistor. This would increase the frequency of oscillation. With the frequency of oscillation a function of the load, power transformer design optimization would be impossible, high losses being the direct result. If the secondaries of T1 were connected directly to the base-emitters of Q1 and Q2, the frequency would almost be constant. The base-emitter voltage would then be the frequency determining voltage. The base-emitter voltage changes very little with base current once the transistor is drawing significant base current. This connection was attempted. The problem encountered here was that slight differences in the base-emitter voltage of the two switching transistors (Q1 and Q2) caused the waveform to be asymetrical with respect to time since T1 saturated in different time intervals on each half-cycle. This caused large current spikes to be drawn by that transistor that was on slightly more than 50% of the time. Diodes D1 and D2 added a voltage drop, which is almost independent of base current, and is common to both half-cycles. Thus, the total drop across the secondaries of T2 is increased. For a fixed voltage difference between the base-emitter voltages of Q1 and Q2, the percentage difference across T1 for each half-cycle is reduced and the problem due to asymetry was essentially eliminated.

Actual operation of the circuit was not very satisfactory. The major problem with the circuit is that the boost oscillator switches a short time (3 to 4μs) after the main oscillator has switched. This switching circuit operated in the following manner. T1 saturates removing drive power from Q1 (or Q2). Q1 remains on for a time equal to its storage time. During this time, since Q1 is still on, T2 is continually supplying full base drive to Q3 (or Q4). When Q1 has been depleted of base charge, it turns off and the main oscillator

begins to switch. Q3 does not turn off immediately as its base drive is removed only when Q1 begins to turn off. Thus, the boost oscillator switching will follow the main oscillator by approximately the storage time of Q3. This seriously affects the switching action of the main oscillator. The instant after the main oscillator switches, the boost oscillator is out-of-phase with the main oscillator instead of in-phase since it has not switched yet. The total secondary voltage (the algebraic sum of the secondary voltages of the main and boost oscillators) is thus considerably less than the output voltage which is maintained by C2 during switching. Thus, the main oscillator is looking into an open circuit since the rectification diodes are reverse biased. A current feedback oscillator will not function into an open circuit load. Therefore, Q2 must be turned on by the starting resistor after the boost oscillator has switched. This "re-starting" every half-cycle caused considerable ringing in the waveform and resulted in excessive switching losses. In an attempt to correct this problem and minimize the phase shift between the two oscillators, the following modification is currently being studied. See Figure 7.

T2 is a non-saturating one-to-one transformer. T2 simply reflects into the secondaries of T1 to the base-emitter of either Q3 or Q4 in series with the base-emitter of Q1 or Q2. When T1 saturates, the drive current is simultaneously removed from Q1 and Q3 (or Q2 and Q4). Thus, the storage interval occurs at the same time for both oscillators. A low impedance path is still available to turn off the switching transistors. When T1 saturates, it represents a short circuit back to the negative end of C1. Charge flowing out of the base of Q1 must flow through the primary of T2. This is a low impedance since the base-emitter of Q3 represents a short circuit on the secondary of T2 during the period of charge-storage immediately prior to turn off. To the extent that the

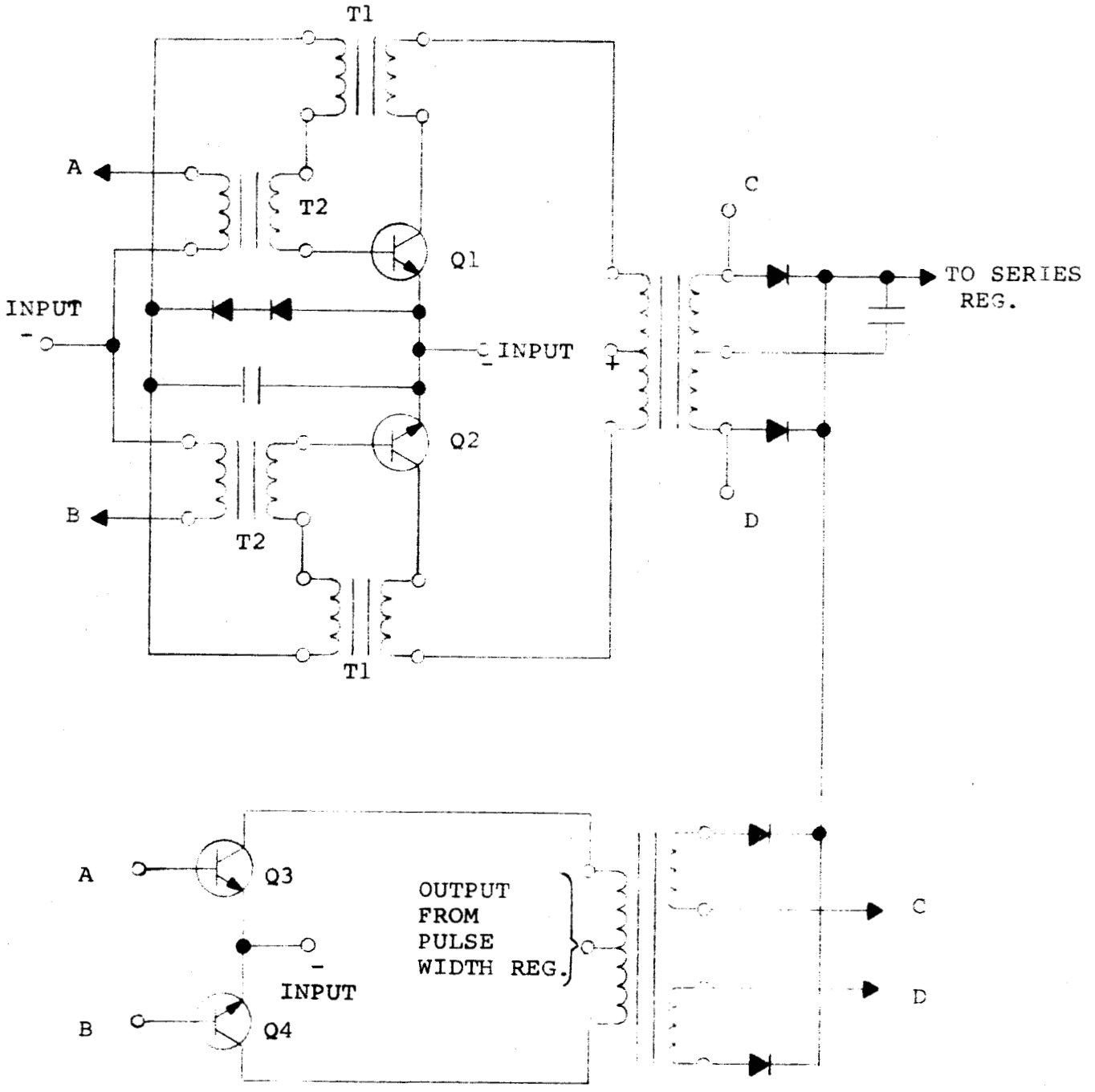
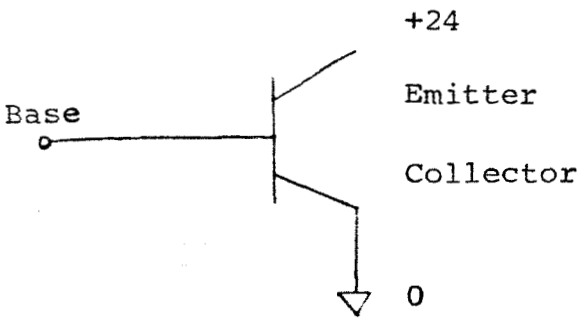


FIGURE 7. MODIFIED MAIN AND BOOST OSCILLATOR CIRCUIT OF APPROACH 5.

coulomb storage is equal in the two transistors, both transistors would be turned off with a strong reverse base current. This circuit is still undergoing investigation but has already proved to be much better than the first method.

One of the largest sources of loss in the unit is in converting the transformer AC output to DC. If diodes are used, there is no possible way of avoiding the loss due to the forward drop during conduction. Another very important source of loss in the diodes is due to the recovery time. If the switching time of the oscillator is appreciably faster than the recovery time of the diodes, and since the turn on time of a diode is essentially instantaneous, both diodes will be on together for a period of time equal to the recovery time immediately after the oscillator has switched. During this period of time, the secondary winding is essentially short circuited, resulting in a power loss. The extent of the problem was illustrated by using two different diodes in the same circuit. The square wave to be rectified had a rise time of 0.4μs. Silicon fast recovery diodes (Hughes HF9D) were first used. Afterward, the base-collector junctions of moderately fast germanium power transistors (Bendix 2N1653) were used as diodes. The drop across the silicon diodes during conduction was 0.9 volts, while that of the germanium diodes was 0.4 volts. Contrary to expectation, the rectification losses were equal in the two cases. Higher peak currents were drawn during switching with the germanium diodes. The change in loss due to recovery time, exceeded the change in loss due to forward drop. An extensive effort has been made to find a suitable transistor to use as a synchronous rectifier. The requirement for this transistor that eliminates many available transistors is that it must have a base-emitter back-voltage rating slightly greater than twice the desired DC output voltage. This can be readily appreciated when it is realized that, like a diode, the transistor must see twice the output voltage in the reverse direction when it is in the off condition. For an NPN transistor, the voltages for a 12 volt output across the off

transistor would be the following:



If the base is at a higher voltage(more positive) than the collector, the transistor will operate in the inverted mode and conduct current from emitter to collector. The base must be more negative than the collector to insure that the transistor is off. Since the collector is already more negative than the emitter by twice the output voltage, the base must be more negative than the emitter by slightly more than twice the output voltage. The only transistors that could be found with a Vebo rating of 25 volts or greater were germanium alloy and slow silicon transistor types. The slow speed of the germanium transistor (Philco type 2N671) would require special drive circuitry to prevent excessive losses due to long recovery times. The undesirability of germanium plus additional complexity of the circuitry makes this approach of questionable value. The silicon transistor that is being considered is type 2N1016. The problems with this type transistor are the high saturation resistance, the high base-emitter forward voltage and the moderate Beta's. These problems combine to give almost no advantage over using diodes. Again, special drive circuitry would be needed to compensate for slow speed.

There is one other possibility for using transistors for rectification. Since the transistors see only the saturation voltage in the forward direction, the base-collector

breakdown voltage (V_{cbo}) need be only one or two volts. Thus, if a high frequency transistor could be found with a good inverse Beta (greater than 10), the transistor could be used in the inverse connection. The high reverse voltage would then appear across the base-collector junction rather than the base-emitter junction. Another advantage to the inverse connection is that the collector-emitter saturation voltage is considerably smaller. However, available high frequency power transistors show Beta's of one or two at the desired current levels in the inverse connection. At this time, there appears to be no suitable substitute for fast recovery diodes for rectification.

B. Components.

Little work has been done on the selection of non-magnetic components. The power switching transistors being used in the saturable core oscillators are silicon-high frequency passivated planar, Minneapolis-Honeywell type 2N2812. Little efficiency is lost in the use of silicon transistors for switching as compared to germanium since the base drive voltage has to be boosted anyway to eliminate asymetry in the squarewave and the saturation resistance is low (about 0.04 ohms). Also, the higher frequency of these transistors results in lower switching losses than in a lower speed germanium transistor. It is EM's understanding at this time that Minneapolis-Honeywell is currently developing a non-magnetic package for this transistor. Power diodes will be of a fast recovery type such as Hughes HF9D or the new Westinghouse 379 series. All low level transistors and diodes will be high frequency silicon devices. Little effort has been expended towards the selection of components other than semiconductors.

III. PROPOSED PROGRAM FOR NEXT REPORTING PERIOD.

The first part of the next period will be expended in the completion of circuitry to properly synchronize the main and boost oscillators. Subsequent to this, the current limiting

circuitry and output series regulators will be designed. This will essentially complete the design except for input filtering considerations. This work will probably require most of the succeeding periods of work. At the completion of the next period, quantitative results can be determined and refinements can be accomplished. During the next period, effort will be continued toward finding a transistor which is suitable for use as a synchronous rectifier. As it becomes known that certain components will definitely be used in the final design, preliminary investigation will begin to determine what will be necessary to obtain these components in a non-magnetic configuration.